

Appl. No. 10/708,373  
Amdt. dated Aug. 03, 2005  
Reply to Office action of May 06, 2005

### AMENDMENTS TO THE CLAIMS

Claim 1 (Currently amended): A multi-stage delay clock generator comprising:

- 5 a plurality of delay cells, each delay cell generating a delay signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal where a first delay cell among the plurality of delay cells receives an external clock signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell;
- 10 a phase detector, responsive to the external clock signal and a feedback clock signal, for generating a lock control signal; and
- ~~an integrator, responsive to the lock control signal, for generating the delay control signal; and~~
- a control unit, responsive to the lock control signal, for generating the delay control signal for programming the delay cells.

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Claim 2 (currently amended): The multi-stage delay clock generator in claim 1, wherein the ~~integrator~~ control unit comprises:

- 20 a delay counter, responsive to the lock control signal, for generating the delay control signal;
- a plurality of multiplexers, responsive to the delay control signal, for outputting a select signal; and
- a plurality of latches, responsive to the select signal, for outputting a lock signal to the plurality of delay cells and to a subsequent multiplexer.

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Claim 3 (original): The multi-stage delay clock generator in claim 1, wherein a range of the first delay cell is greater than a range of a maximum delay target from the external clock signal.

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Claim 4 (original): The multi-stage delay clock generator in claim 1, wherein the delay step of a last delay cell is smaller than a system jitter.

- 5    Claim 5 (original): The multi-stage delay clock generator in claim 1, wherein a delay step of the first delay cell is determined by a total number of programming bits.

10    Claim 6 (original): The multi-stage delay clock generator in claim 5, wherein the total number of programming bits is a value from dividing the range of the maximum delay target by the delay step of the first delay cell.

Claim 7 (original): The multi-stage delay clock generator in claim 1, wherein a number of delay cells is dependent on a resolution of the last delay cell.

- 15    Claim 8 (original): The multi-stage delay clock generator in claim 1 further comprises a delay offset electrically coupled to a last delay cell for generating an offset delay signal.

20    Claim 9 (original): A method for generating a delay signal comprising:  
comparing an external clock signal and a feedback to determine a maximum delay target;  
dividing a first delay cell into a plurality of delay steps according to a number of programming bits that is obtained from the maximum delay target;  
repeatedly dividing a subsequent delay cell into a plurality of smaller delay steps  
25    according to a size of the delay steps of the first delay cell, wherein each subsequent delay cell comprises smaller and smaller delay steps;  
comparing the external clock signal to the delay step of the delay cells by a tunable detecting window to output a lock control signal;

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latching the delay cell according to the lock control signal;  
adjusting a width of the tunable detecting window for the subsequent delay cells;  
and  
sending a delay control signal to the delay cells.

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Claim 10 (original): The method of claim 9 further comprises initially programming the delay cells.

Claim 11 (original): The method of claim 10, wherein initially programming the delay  
10 cells comprises:

asserting a reset signal to the first delay cell;  
calibrating the first delay cell;  
latching a delay value of the first delay cell; and  
asserting the reset signal to the subsequent delay cell until all delay cells are  
15 calibrated.

Claim 12 (original): The method of claim 9, wherein a delay step of the first delay cell is determined by a total number of programming bits.

20 Claim 13 (original): The method of claim 9 further comprises a delay offset electrically coupled to a last delay cell for generating an offset delay signal used for preventing a trap causing lock-failure.

Claim 14 (currently amended): A multi-stage delay clock generator for generating a delay  
25 signal, comprising:  
a first delay chain for generating a first delay signal, in response to an external clock signal and a first delay control signal, comprising a plurality of delay cells, each delay cell generating a delayed clock signal from a preceding delay cell and a

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- delay control signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell;
- 5 a second delay line chain for generating a second delay signal, in response to a second delay control signal and a feedback clock signal, comprising a plurality of delay cells, each delay cell generating a delayed clock signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell;
- 10 a first phase detector, responsive to a delayed external clock signal and the first delay signal, for generating a first control signal;
- a second phase detector, responsive to a delayed feedback clock signal and the second delay signal, for generating a second control signal; and
- ~~an integrator, responsive to the first and the second control signal, for generating the first delay control signal and the second delay control signal; and~~
- 15 a control unit, responsive to the first and the second control signal, for generating the first delay control signal and the second delay control signal for programming the delay cells.

- Claim 15 (currently amended): The multi-stage delay clock generator in claim 14,
- 20 wherein the ~~integrator~~ control unit comprises:
- a delay counter, responsive to the lock control signal, for generating the delay control signal;
- a plurality of multiplexers, responsive to the delay control signal, for outputting a select signal; and
- 25 a plurality of latches, responsive to the select signal, for outputting a lock signal to the plurality of delay cells and to a subsequent multiplexer.